REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added changes in accordance with NOR 5962-R116-94.	94-03-03	M. A. Frye
B	Added 03 device, removed CAGE number 01295, and made editorial changes throughout.	96-07-09	M. A. Frye

REV																				
SHEET																				
REV	B	B	B	B	B	B														
SHEET	15	16	17	18	19	20														

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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CHECKED BY
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APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
93-04-07

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY, 8000 GATES, MONOLITHIC SILICON

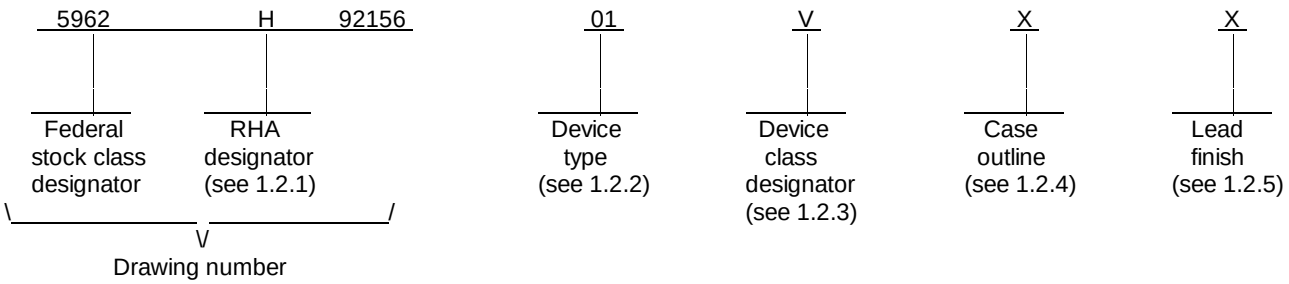
SIZE	CAGE CODE	
A	**67268**	**5962-92156**

SHEET 1 OF 20

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-PRF-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
01	1280	8000 gate field programmable gate array	251 ns
02	1280-1	8000 gate field programmable gate array	218 ns
03	RH1280	8000 gate field programmable gate array	160 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA7 - P176	176	Pin grid array
Y	See figure 1	172	Flat pack
Z	CMGA7 - P176	177	Pin grid array with orientation pin

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-PRF-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

DC supply voltage range (V_{DD})	-0.5 V dc to +7.0 V dc
Input voltage range (V_I)	-0.5 V dc to V_{DD} + 0.5 V dc
Output voltage range (V_O)	-0.5 V dc to V_{DD} + 0.5 V dc
Input clamp current (I_{IC})	±20 mA
Output clamp current (I_{OC})	±20 mA
Continuous output current (I_O)	±25 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (Θ_{JC}) :	
Case X and Z	See MIL-STD-1835
Case Y	10°C/W 2/
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Radiation: Total dose	300K rads (maximum) 3/

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.

3/ Device electrical characteristics are guaranteed for post irradiation levels at 25°C, in low dose rate environment (post 168 hours, 100°C, biased anneal).

4/ 100 percent test coverage of blank programmable logic devices.

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s).

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or quality conformance inspection group A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of logic modules shall be utilized or at least 25 percent of the total logic modules shall be utilized for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be as specified on figure 4.

3.2.5 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device classes M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures on a minimum of ten worst case pins from each device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Devices shall be tested for programmability and ac performance compliance to the requirements of Group A, subgroups 1 and 7. Either of two techniques is acceptable.

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 1 and 7, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2a) If such compliance cannot be tested on as unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 1 and 7. Eight devices shall be submitted to programming (see 3.2.3.2). If any device fails to program the lot shall be rejected. At the manufacturer's option, the sample may be increased, but must comply with a LTPD of 30. For radiation hardened devices, should any lot fail the programming sample, a failure analysis and TRB disposition are required.

(2b) Eight devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9 for binning circuit delay only. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased, but must comply with a LTPD of 30. For radiation hardened devices, should any lot fail the programming sample, a failure analysis and TRB disposition are required.

(2c) If the binning circuit is tested on 100 percent of the products, then the above requirement is met.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H. RHA levels for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 if MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	Test one output at a time, $V_{DD} = 4.5\ V$, $I_{OH} = -3.2\ mA$	1, 2, 3	All	3.7		V
Low level output voltage	V_{OL}	Test one output at a time, $V_{DD} = 4.5\ V$, $I_{OL} = 4.0\ mA$	1, 2, 3	All		0.4	V
Low level input voltage	V_{IL}		1, 2, 3	All	-0.3	0.8	V
High level input voltage	V_{IH}		1, 2, 3	01,02	2.0	V_{CC} +0.3	V
				03	2.2	V_{CC} +0.3	
Standby supply current	I_{DD}	Outputs unloaded, $V_{DD} = 5.5\ V$, $V_{IN} = V_{DD}$ or GND	1, 2, 3	All		25	mA
Input leakage current	I_{IL}	$V_{DD} = 5.5\ V$, $V_{IN} = V_{DD}$ or GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	$V_{DD} = 5.5\ V$, $V_O = V_{DD}$ or GND	1, 2, 3	All	-10	10	µA
I/O terminal capacitance	$C_{I/O}$	See 4.4.1c, f= 1.0 Mhz, $V_{OUT} = 0\ V$	4	All		20	pF
Functional tests	FT 2/	See 4.4.1eV, $V_O = 0\ V$	7, 8A, 8B	All			
Binning circuit delay	t_{PBLH}, t_{PBHL}	See figure 3, $V_{IL} = 0\ V$, $V_{IH} = 3.0\ V$, $V_{DD} = 4.5\ V$, $V_{OUT} = 1.5\ V$ 3/	9, 10, 11	01		251	ns
				02		218	
				03		160	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

1/ All tests shall be performed under the worst case condition unless otherwise specified. Devices supplied to this drawing will meet levels M, D, L, R, and F, of irradiation. However, this device is only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electriclal measurements for any RHA level, T_A = +25°C.

2/ Devices are functionally tested using a serial scan test method. Data is shifted into the SDI pin and the DCLK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the PRA, PRB or SDO pins. These tests form a part of the manufacturers's test tape and shall be maintained and available at the approved source(s) of supply upon request by DESC or the OEM.

3/ Binning circuit delay is defined as the input-to-output delay of a special path called the "binning circuit". The binning circuit consists of one input buffer plus 16 combinatorial logic modules plus one output buffer. The logic modules are distributed along the left side of the device. These modules are configured as non-inverting buffers and are connected through programmed antifuses with typical capacitive loading.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

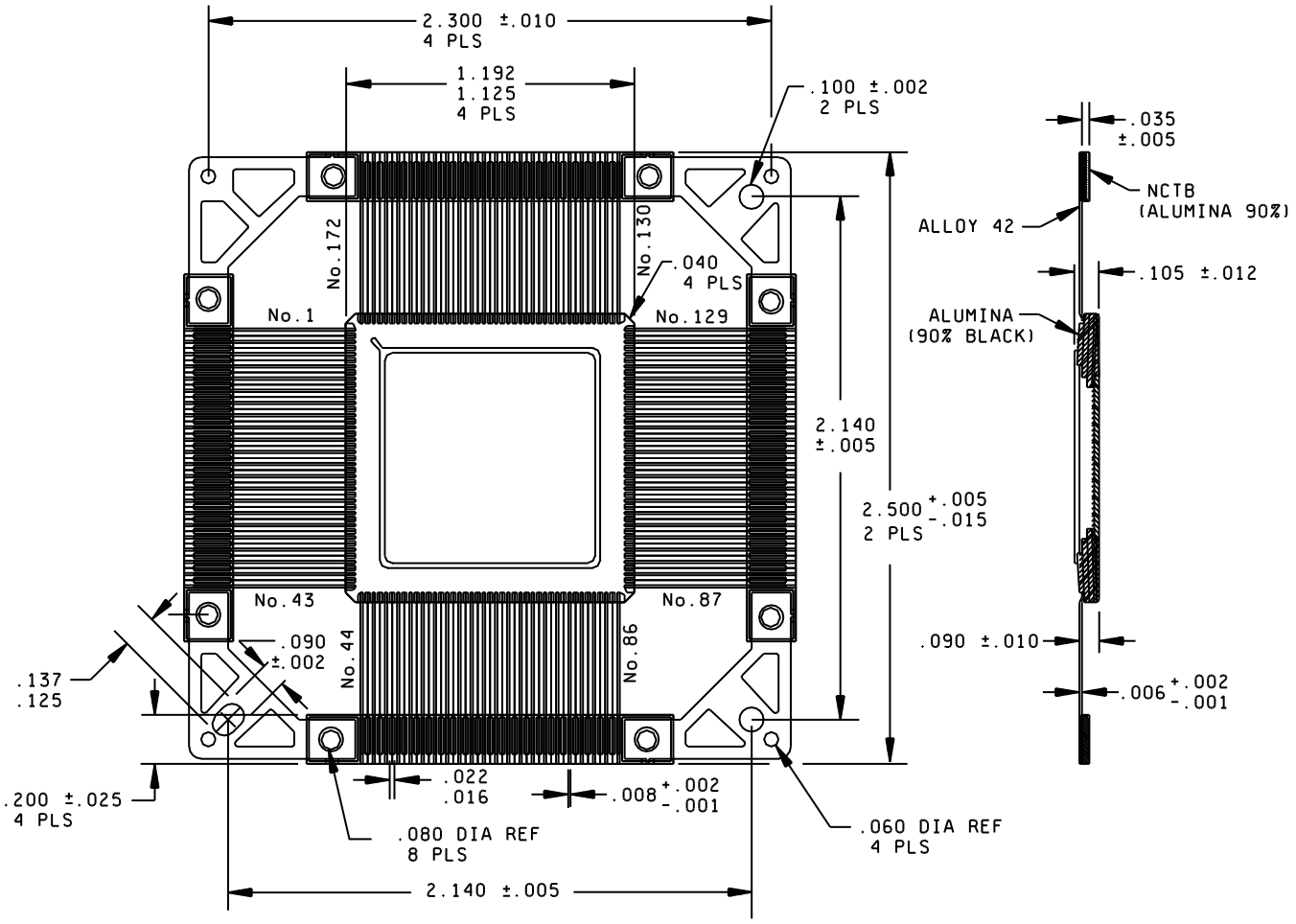
f. Bias conditions shall be V_{DD} = 4.5 V dc for the upset measurements and V_{DD} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see Table IB herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

Case Y



NOTES:
1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 µ mm) min. thickness over 80 to 350 microinches (2.0 to 8.9 µ mm) thickness of nickel.
2. Seal ring area is connected to GNDA.
3. Die attach pad is connected to GNDA.
4. GNDQ (4 PLS) is connected to GNDA.
5. Tolerances unless otherwise specified: ± 1% N.L.T ± 0.005.

FIGURE 1. Case outline.

Case Y

Inches	mm	Inches	mm
.001	0.03	.080	2.03
.002	0.05	.090	2.29
.005	0.13	.100	2.54
.006	0.15	.105	2.67
.008	0.20	.125	3.18
.010	0.25	.137	3.48
.012	0.30	.200	5.08
.015	0.38	1.125	28.58
.016	0.41	1.192	30.28
.018	0.46	2.140	54.36
.022	0.56	2.300	58.42
.025	0.64	2.500	63.50
.035	0.89		
.040	1.02		
.060	1.52		
.067	1.70		

NOTE: Metric equivalents are for reference only.

FIGURE 1. Case outline - Continued.

Case outlines X and Z

Device type	All		Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
A1	I/O		D1	I/O		H1	I/O		M13	I/O
A2	I/O		D2	I/O		H2	VSV		M14	I/O
A3	I/O		D3	I/O		H3	V_{DD}		M15	I/O
A4	I/O		D4	GND		H4	GND		N1	I/O
A5	I/O		D5	V_{DD}		H12	GND		N2	I/O
A6	IN		D6	GND		H13	V_{DD}		N3	I/O
A7	IN		D7	PRB or I/O		H14	VSV		N4	I/O
A8	IN		D8	V_{DD}		H15	I/O		N5	I/O
A9	CKA or I/O		D9	I/O		J1	I/O		N6	I/O
A10	I/O		D10	GND		J2	I/O		N7	I/O
A11	I/O		D11	V_{DD}		J3	I/O		N8	V_{DD}
A12	I/O		D12	GND		J4	V_{DD}		N9	I/O
A13	I/O		D13	I/O		J12	GND		N10	I/O
A14	I/O		D14	I/O		J13	VKS		N11	I/O
A15	I/O		D15	I/O		J14	VPP		N12	I/O
B1	GND		E1	I/O		J15	I/O		N13	I/O
B2	I/O		E2	I/O		K1	I/O		N14	I/O
B3	DCK or I/O		E3	I/O		K2	I/O		N15	I/O
B4	I/O		E4	GND		K3	I/O		P1	I/O
B5	I/O		E5	GND 1/		K4	GND		P2	I/O
B6	GOE		E12	GND		K12	GND		P3	I/O
B7	GND		E13	I/O		K13	I/O		P4	I/O
B8	CKB or I/O		E14	I/O		K14	I/O		P5	I/O
B9	I/O		E15	I/O		K15	I/O		P6	I/O
B10	I/O		F1	I/O		L1	I/O		P7	I/O
B11	I/O		F2	I/O		L2	I/O		P8	I/O
B12	GND		F3	I/O		L3	I/O		P9	I/O
B13	I/O		F4	V_{DD}		L4	GND		P10	I/O
B14	SDI or I/O		F12	GND		L12	I/O		P11	I/O
B15	I/O		F13	I/O		L13	I/O		P12	I/O
C1	I/O		F14	I/O		L14	I/O		P13	SDO or I/O
C2	I/O		F15	I/O		L15	I/O		P14	I/O
C3	MODE		G1	I/O		M1	I/O		P15	I/O
C4	I/O		G2	I/O		M2	I/O		R1	I/O
C5	I/O		G3	I/O		M3	I/O		R2	I/O
C6	I/O		G4	GND		M4	GND		R3	I/O
C7	I/O		G12	V_{DD}		M5	V_{DD}		R4	I/O
C8	GND		G13	I/O		M6	GND		R5	I/O
C9	PRA or I/O		G14	I/O		M7	I/O		R6	I/O
C10	I/O		G15			M8	GND		R7	I/O
C11	I/O					M9	I/O		R8	I/O
C12	I/O					M10	GND		R9	I/O
C13	I/O					M11	V_{DD}		R10	I/O
C14	I/O					M12	GND		R11	I/O
C15	I/O								R12	I/O
									R13	I/O
									R14	I/O
									R15	I/O

1/ E5 is an orientation pin that is available on package Z only.

FIGURE 2. Terminal connections.

Case outline Y

Device type	All		Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	MODE		51	I/O		101	I/O		151	VDD
2	I/O		52	I/O		102	I/O		152	GND
3	I/O		53	I/O		103	GND		153	I/O
4	I/O		54	I/O		104	I/O		154	CKB or I/O
5	I/O		55	GND		105	I/O		155	I/O
6	I/O		56	I/O		106	VKS		156	PRB or I/O
7	GND		57	I/O		107	VPP		157	I/O
8	I/O		58	I/O		108	GND		158	I/O
9	I/O		59	I/O		109	VDD		159	I/O
10	I/O		60	I/O		110	VSV		160	I/O
11	I/O		61	I/O		111	I/O		161	GND
12	VDD		62	I/O		112	I/O		162	I/O
13	I/O		63	I/O		113	VDD		163	I/O
14	I/O		64	I/O		114	I/O		164	I/O
15	I/O		65	GND		115	I/O		165	I/O
16	I/O		66	VDD		116	I/O		166	VDD
17	GND		67	I/O		117	I/O		167	I/O
18	I/O		68	I/O		118	GND		168	I/O
19	I/O		69	I/O		119	I/O		169	I/O
20	I/O		70	I/O		120	I/O		170	I/O
21	I/O		71	I/O		121	I/O		171	DCK or I/O
22	GND		72	I/O		122	I/O		172	I/O
23	VDD		73	I/O		123	GND			
24	VSV		74	I/O		124	I/O			
25	I/O		75	GND		125	I/O			
26	I/O		76	I/O		126	I/O			
27	VDD		77	I/O		127	I/O			
28	I/O		78	I/O		128	I/O			
29	I/O		79	I/O		129	I/O			
30	I/O		80	VDD		130	I/O			
31	I/O		81	I/O		131	SDI or I/O			
32	GND		82	I/O		132	I/O			
33	I/O		83	I/O		133	I/O			
34	I/O		84	I/O		134	I/O			
35	I/O		85	SDO or I/O		135	I/O			
36	I/O		86	I/O		136	VDD			
37	GND		87	I/O		137	I/O			
38	I/O		88	I/O		138	I/O			
39	I/O		89	I/O		139	I/O			
40	I/O		90	I/O		140	I/O			
41	I/O		91	I/O		141	GND			
42	I/O		92	I/O		142	I/O			
43	I/O		93	I/O		143	I/O			
44	I/O		94	I/O		144	I/O			
45	I/O		95	I/O		145	I/O			
46	I/O		96	I/O		146	I/O			
47	I/O		97	I/O		147	I/O			
48	I/O		98	GND		148	PRA or I/O			
49	I/O		99	I/O		149	I/O			
50	I/O		100	I/O		150	CKA or I/O			

FIGURE 2. Terminal connections - Continued.

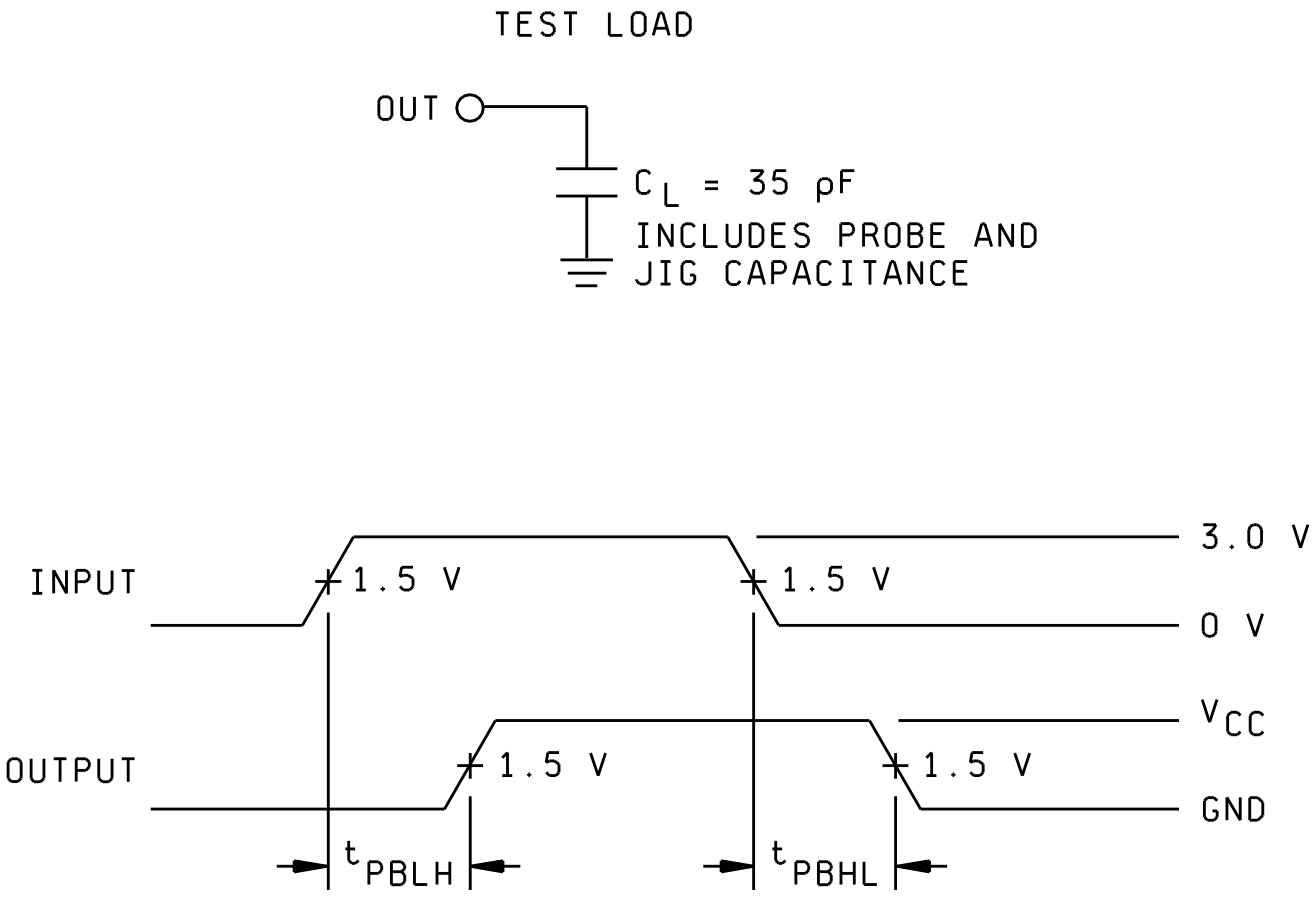
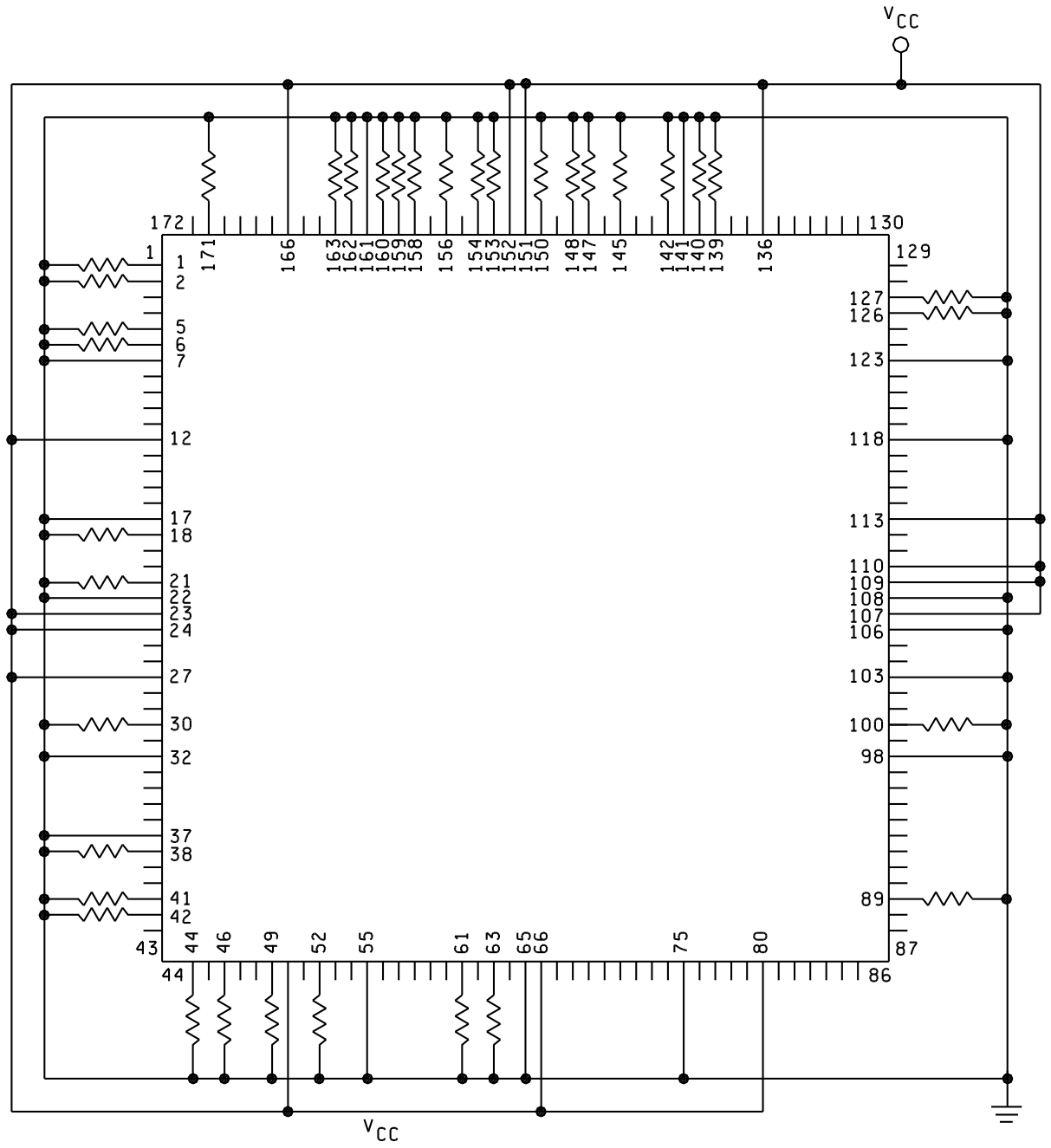


FIGURE 3. Switching test circuit and waveforms.



Note: Resistors are 1kΩ resistors.

FIGURE 4. Radiation exposure circuit.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-92156
		REVISION LEVEL B	SHEET 16

TABLE IB. SEP test limits. 1/

Symbol	Characteristics	Logic Modules	Conditions	Bias V_{CC} =	Effective LET no upset/latchup (MeV-cm^2/mg)	Maximum device cross section μm^2/bit LET = 120
SEL	Single event latchup	All	$55°C \le T_{case} \le 125°C$	5.5 V	177	N/A
SEU	Single event upset	Combinatorial	$55°C \le T_{case} \le 125°C$	4.5 V	17	320
		Sequential	$55°C \le T_{case} \le 125°C$	4.5 V	4	110
SEDR 2/	Single event dielectric (antifuse) rupture	N/A	$55°C \le T_{case} \le 125°C$	5.5 V	60 2/	N/A

1/ Verification test per TRB approved test plan.
2/ Tested with ions having perpendicular incidence, cross section < 0.002um^2/antifuse at LET = 60 MeV-cm^2/mg.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-PRF-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7*, 9 Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7*, 9 Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A,8B	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

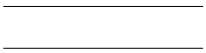
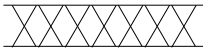
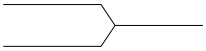
TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{DD}	±10% of specified value of table IA
I_{IL}	±10% of specified value of table IA
I_{OZ}	±10% of specified value of table IA
t_{PBLH}, t_{PBHL}	±10 ns

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-PRF-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-PRF-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.7 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-07-09

Approved sources of supply for SMD 5962-92156 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar 2/ PIN
5962-9215601MXC	0J4Z0 0J4Z0	A1280A PG176B TPC1280MGB176B
5962-9215601MYC	0J4Z0 0J4Z0	A1280A CQ172B TPC1280MHFG172B
5962-9215601MZC	0J4Z0 0J4Z0	A1280A CQ177B TPC1280MGB177B
5962-9215602MXC	0J4Z0 0J4Z0	A1280A-1 PG176B TPC1280MGB176B-1
5962-9215602MYC	0J4Z0 0J4Z0	A1280A-1 CQ172B TPC1280MHFG172B-1
5962-9215602MZC	0J4Z0 0J4Z0	A1280A-1 CQ177B TPC1280MGB177B-1
5962F9215603QYC	0J4Z0	RH1280-CQ172V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0J4Z0	Actel Corporation 955 East Arques Ave. Sunnyvale, CA 94086